Nb/Al-Al_2O_3/Nb Junctions with Inductive Tuning Elements for a Very Low Noise 205–250 GHz Heterodyne Receiver

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Abstract—**The superconductor-insulator-superconductor (SIS) junction is the most sensitive nonlinear element for millimeter-wave heterodyne detection. We have developed a Nb/Al-Al_2O_3/Nb junction fabrication process which allows the use of planar tuning circuits integrated with the junctions. These tuning elements permit the use of junctions with relatively large areas and small current densities with excellent results. Recent measurements have yielded a double sideband receiver noise temperature less than 50K from 205 to 240 GHz and 44K at 230 GHz. We are also extending our Nb/Al-Al_2O_3/Nb trilayer technology to the fabrication of sub-square-micron area planar junctions for submillimeter wavelengths.**

I. Introduction

Nb/Al-Al_2O_3/Nb trilayer junctions have surpassed those made by all other SIS technologies in leakage current and uniformity. They are currently the element of choice for ultra low noise millimeter wave heterodyne detection. We are investigating both Nb and NbCN superconductors in the planar and edge junction geometries for millimeter and submillimeter wavelengths. In this paper we discuss the recent results of our Nb trilayer technology.

There have generally been two approaches to optimizing SIS mixers for millimeter wavelengths: 1) the use of very small area, high current density (J_c) junctions to minimize $\omega R_N C$ [1]–[5], where R_N is the normal state resistance and C is the junction capacitance, and 2) the use of integrated elements to tune out the junction capacitance while keeping the benefits of a larger junction capacitance [6]–[11]. For millimeter wavelength, both approaches have been rather successful. At higher frequencies the use of increasingly smaller junction areas and higher J_c values may be restricted by fabrication limitations and the properties of available superconductors. For example, with $C_s = 45$ fF/μm^2, $I_C R_N = 1.8$ mV, and $R_N = 100\ \Omega$ [12], a choice of $\omega R_N C = 1$ at 100 GHz with the Nb/Al-Al_2O_3/Nb system requires a junction area of approximately 0.35 μm^2 and a $J_c = 5.1 \times 10^3$ A/cm^2. Even if we ignore the $J_c \propto f^2$ relationship found by Kerr and Pan for the choice of $\omega R_N C = 4$ [10], at 600 GHz and 1 THz the desired junction areas and J_c values would still be 0.06 μm^2 and 3×10^4 A/cm^2, and 0.035 μm^2 and 5×10^4 A/cm^2, respectively. In light of the analysis by Kerr and Pan, these numbers, particularly the J_c values, are certainly optimistic estimates. The fabrication of such planar trilayer junctions having reasonable electrical characteristics may be quite difficult. An attractive alternative is the use of integrated superconductive tuning elements and impedance matching superconductive transmission lines, which permit the use of larger junction areas and smaller J_c values (larger $\omega R_N C$). Additionally, the expected difficulty in suppressing Josephson currents (and the resulting Josephson noise) for very small junction areas and arrays of junctions argues for the integrated tuning element approach. Resistive loss in superconductor films at frequencies approaching $2\Delta/h$ ($\approx$700 GHz for Nb) will, however, prevent the use of superconductive tuning elements above these frequencies, and normal metal tuning elements [9] or alternative mixer designs will need to be developed.

II. SIS Mixer Elements with Integrated Tuning Elements

For SIS mixers, the use of relativity large $\omega R_N C$ values has three advantages: (i) The large capacitance tends to short-circuit currents at the LO harmonics and harmonic sidebands, (ii) Undesired effects of the AC Josephson currents in the junction are reduced, and (iii) It is easier to fabricate the required junction elements. However, for good mixer performance it is necessary to tune out the junction capacitance at the signal frequency. To do this, we have used inductive tuning circuits integrated with the individual junctions [9], [12], [13]. In our earlier work [9], [13], we reported utilizing a trilevel resist to pattern junction areas in Nb/Al-Al_2O_3/Nb films and to define the inductive portion of the stripline tuning element (Fig. 1). After reactive ion etching to define the junction area, the perimeter of the junction is revealed and a liftoff structure is defined with an oxygen plasma shrink of the exposed polyimide sidewalls. A subsequently off-axis de-

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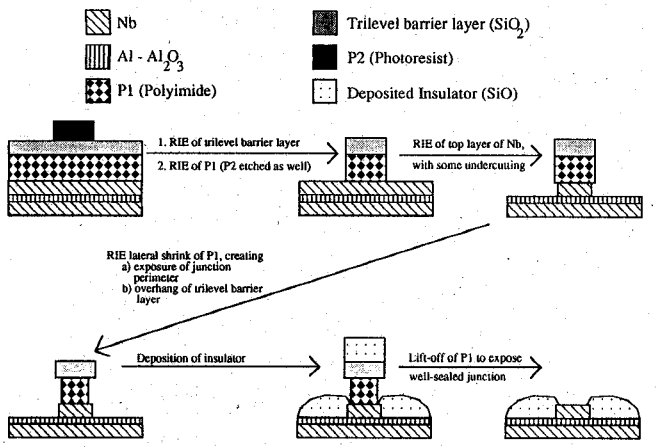

Fig. 1. Outline of original trilevel resist insulation process.

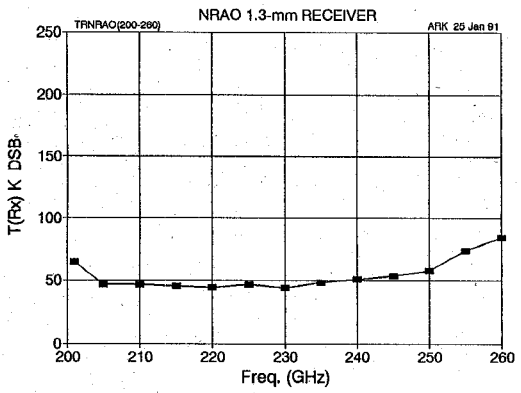

Fig. 2. Noise temperature measurements from 205 GHz to 260 GHz for a NRAO receiver incorporating Nb/Al-Al_2O_3/Nb junctions fabricated at the University of Virginia. The DSB receiver noise temperature at 230 GHz was 44K.

posited insulation layer seals the sides and the perimeter of the Nb counter electrode button and forms the dielectric for the inductive superconductive stripline. The excellent liftoff profile that is obtained with this technique allows the use of thick insulation layers. We have utilized this technique repeatably to fabricate high-quality junctions of 1.5 μm diameter and current density as large as 1×10^4 A/cm^2.

The most recent results at 230 GHz are shown in Fig. 2. A six junction array was mounted in an NRAO-401 mixer which utilizes two non-contacting adjustable tuners positioned in full-height waveguide. The DSB mixer noise temperature and gain at 230 GHz are 15.5K and -1.5 dB respectively. The receiver has a DSB noise temperature (T_R) of 44 K at 230 GHz, and a T_R below 50K from 205 GHz to 240 GHz [14]. These figures are the lowest reported for a receiver operating over this frequency range. The integrated tuning elements permitted the use of junctions which are relatively large (A $\approx .4\mu$m^2) and also have a low current density ($J_c \approx 3 \times 10^3$ A/cm^2).

III. Cr Trilevel Resist Insulation Process

The optimal performance of SIS mixers requires that the junction area be decreased as the frequency of operation increases; however, an isotropic Nb etch limits the present SiO_2 trilevel process to the fabrication of junctions with an area of $\approx 1.5\ \mu$m^2. The limitation arises from an unfortunate characteristic of the SiO_2 masking layer: it etches rapidly in low pressure CF_4 based etches which are otherwise well-suited for anisotropic definition of the Nb counter electrodes. The high pressure (300 μm) Nb etch of the present process appreciably increases lateral etching, or "undercutting," of the Nb counter electrode. The undercutting is especially problematic for small features because the Nb counter electrode is either etched away entirely or is so small that the subsequent oxygen plasma shrink of the polyimide layer to expose the counter electrode perimeter can not be performed repeatably, (Fig. 3).

Our new approach involves the replacement of the SiO_2 with a $\approx$600 Å Cr layer (defined by wet etching) which is resistant to the $CF_4 + O_2$ Reactive Ion Etching (RIE) chemistry. As a result, the Nb counter electrode layer may be etched with a low pressure (25 μm) RIE process which yields no undercutting. In fact, we have determined that if the polyimide features are shrunk *prior* to the low pressure Nb etch, then the Nb etch defines junctions whose sizes are determined by the Cr overhang of each feature rather than by the polyimide. The low pressure etch leaves the Nb untouched beneath the polyimide and only slightly etches the Nb beneath the Cr overhang. Consequently, there is already an exposed top surface along the perimeter of each junction, so no additional polyimide shrink step is necessary before the deposition of the SiO insulation layer. Eliminating the polyimide shrink after the Nb etch is particularly beneficial because difficulties in shrinkage due to Plasma Resist Image Stabilization Technique (PRIST) hardening [9], [15] from the Nb etch are avoided.

This improved approach is depicted in Fig. 4; it should be noted that the polyimide defining etch and polyimide shrink have been combined into a single step. These were combined by decreasing the power density and hence the anisotropy of the initial polyimide etch. Fig. 5 is an SEM micrograph of a 1 μm diameter junction prior to insulator deposition and polyimide liftoff. It is apparent that there is enough exposed area along the perimeter to easily allow sealing of the junction perimeter with an insulator. Fig. 6 shows such a sealed junction after the polyimide liftoff. If wafers were kept stationary during the off-axis deposition of SiO, the Cr overhang would prevent SiO from reaching a portion of each junction perimeter. Thus, in order to allow symmetric coverage of the junction perimeters, the wafer is rotated, resulting in the ring of thinner SiO surrounding each junction.

In Fig. 7, the deposition of SiO has been omitted; however, the polyimide feature has been lifted off to expose an entire junction. In addition to allowing an accurate determination of junction size, such a view also clearly indicates a slight etching of the Nb which was outside the polyimide feature yet beneath the Cr overhang. When the SiO deposition step is included before liftoff, the SiO covers this ring of slightly etched Nb (Fig. 4). Our results

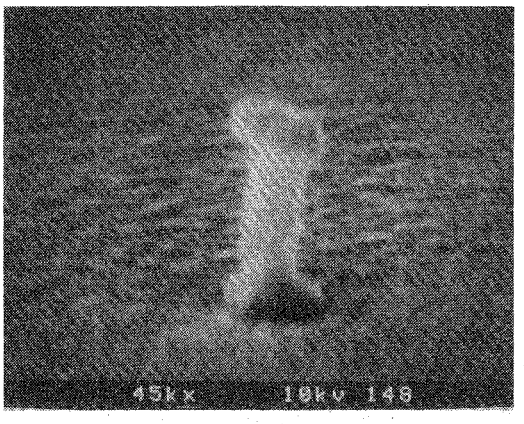

Fig. 3. An SEM micrograph of a 0.3 μm $\times$ 0.3 μm Nb junction area for which a successful SiO_2 based trilevel resist feature was obtained. The shrinkage from the mask feature size of 0.8 μm $\times$ 0.8 μm is primarily due to the "undercutting" of the Nb film in the high pressure $CF_4 + O_2$ etch. A lateral shrinkage of 0.25 μm $< x_{shrink} <$ 0.35 μm was therefore required for this successful polyimide shrink step. This step is performed, however, without quantitative information on the extent of the Nb undercutting, resulting in poor repeatability.

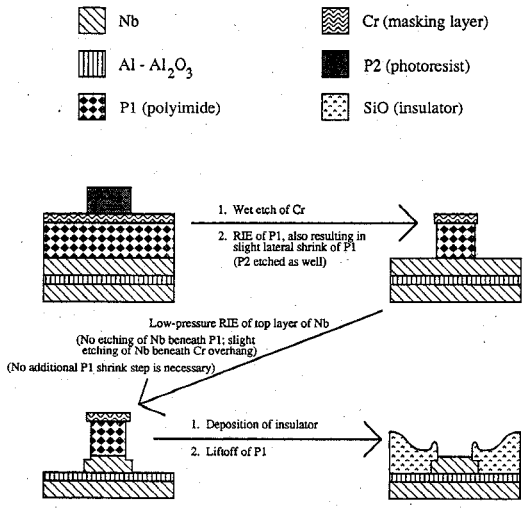

Fig. 4. Improved trilevel resist process featuring CR masking layer.

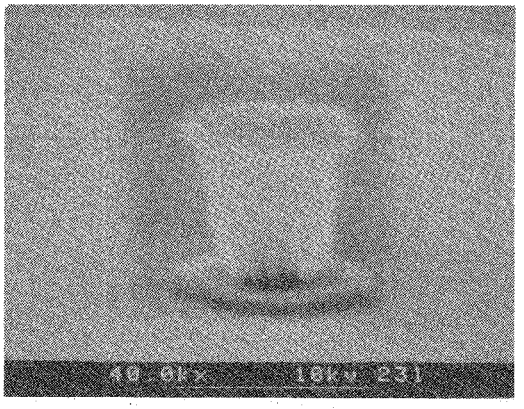

Fig. 5. An SEM micrograph of a Cr based trilevel resist defined Nb counter electrode. The excellent liftoff profile has been obtained with a preshrink of the polyimide *prior* to definition of the junction area. The subsequent SiO deposition will insulate the perimeter of the junction area.

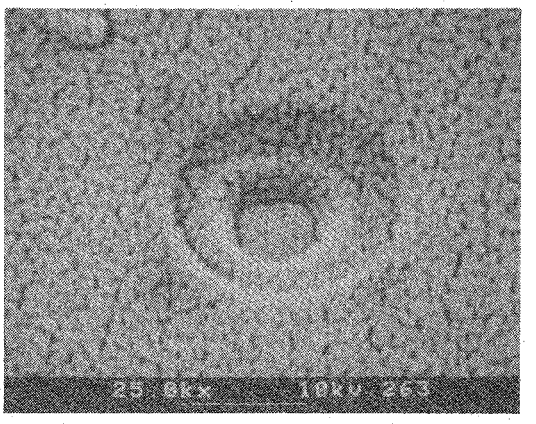

Fig. 6. An SEM micrograph of a Nb counter electrode whose perimeter has been well sealed with SiO using the improved trilevel resist process. (The cracks are in a gold layer deposited on the SEM sample to create a conducting surface.)

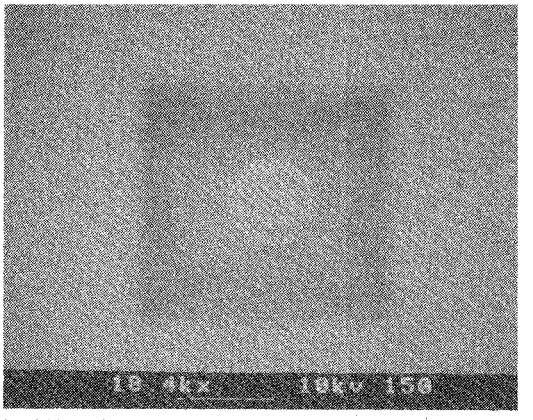

Fig. 7. An SEM micrograph of a 1 μm diameter Nb electrode on a wafer for which the SiO insulation step was omitted.

indicate that the width of this ring varies very little with junction size; thus, junctions of a wide range of sizes should be equally well-sealed along their perimeters. Presently, we have used this Cr-based trilevel resist process to define junction areas as small as 0.5 μm^2.

IV. Summary

SIS mixer elements, based on the Nb/Al trilayer system, have resulted in very low receiver noise temperatures from 205 GHz to 240 GHz. Although other material systems and geometries (the NbN/MgO material system and the edge geometry in particular) appear attractive for submillimeter wavelengths, the Nb/Al trilayer system may prove to be a competitive technology. Our present research with the Nb trilayer system includes new fabrication techniques for sub-square-micron junction areas, and individually tuned and fixed tuned SIS detector elements. In addition to heterodyne detection work, direct detection experiments are ongoing at 585 GHz and 763 GHz.

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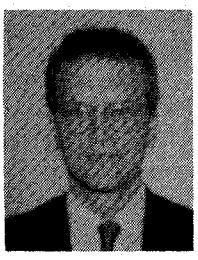

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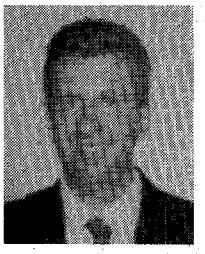

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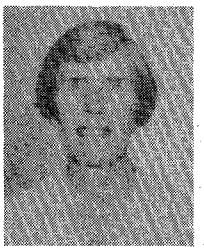

Frances L. Lloyd (nee Frances L. Lummis) received the B.S. degree from Duke University in 1946 and the M.S. degree from the University of Virginia in 1948, both in physics.

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